(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 312 370**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **88309622.4**

(22) Date of filing: **13.10.88**

(51) Int. Cl.[4]: **G 06 F 7/548**
G 06 F 7/60, G 06 F 1/02

(30) Priority: **13.10.87 JP 257556/87**

(43) Date of publication of application:
19.04.89 Bulletin 89/16

(84) Designated Contracting States: **DE FR GB NL**

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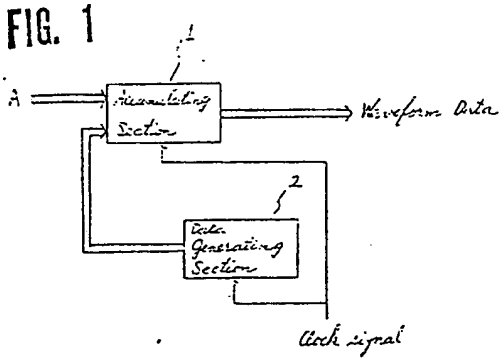
(54) Digital oscillation apparatus.

(57) An apparatus that generates a cyclic waveform of optional multiples of clock frequency in a digital signal processing. The apparatus accumulates a data string having a predetermined average value and a constant with an accumulating circuit which overflows when the data exceeds a dynamic range, thereby to provide cyclic waveform data proportional to the sum of the average value and the constant. Accumulation of the sum of the average value and the constant provides a cyclic waveform of optional multiples of the clock frequency by changing the average value of the data string even if the constant is integer.

FIG. 1



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Description

Digital oscillation apparatus

The present invention relates to a digital oscillation apparatus that generates waveform data representing a periodic waveform having a desired period.

Conventionally, in order to obtain periodic waveform data, an oscillation apparatus that accumulates a specific constant for every clock by use of an adder that overflows when the data exceeds a dynamic range.

This apparatus can vary the period of the generated waveform by varying the value of the constant to be accumulated. However, since it cannot select any value for the constant in the integer operation, the period which can be obtained is limited.

An object of the present invention is to provide a digital oscillation apparatus which generates a periodic waveform data whose period is any rational-number multiple of the clock period.

This object can be achieved by a digital oscillation apparatus which comprises:

data generating means driven by a clock signal having a frequency fc for periodically generating a data string with a repetition period of m clocks (m is integer), the total value of the data string in each repetition period being R (R is integer); and

accumulating means driven by the clock signal and having a dynamic range D (D is integer) for accumulating each data of the data string generated by said data generating means and a constant A (A is integer) until the accumulated result exceeds the dynamic range D, and subtracting the dynamic range D from the accumulated result when the accumulated result exceeds the dynamic range D, thereby generating a periodic waveform data having a frequency fs $(A + \frac{R}{m}) \cdot fc/D$.

FIG. 1 is a block diagram showing a configuration of a first embodiment of the present invention;

FIG. 2 is a waveform diagram showing an output data waveform of the first embodiment of the present invention;

FIG 3 is a block diagram showing a configuration of a second embodiment of the present invention;

FIG. 4 is a block diagram showing a configuration of a third embodiment of the present invention;

FIG. 5 is a block diagram showing a configuration of a fourth embodiment of the present invention;

FIG. 6 is a waveform diagram showing waveform of data stored in a ROM in the fourth embodiment of the present invention; and

FIG. 7 is a block diagram showing a fifth embodiment of the present invention.

In FIG. 1, a digital oscillation apparatus comprises an accumulating section 1 and a data generating section 2. The accumulating section 1 is responsive to a clock signal to accumulate a constant A and an output of the data generating section 2 clock by clock. When the output of the data generating section 2 is constantly zero (0), an output waveform data as shown in FIG. 2 is obtained. That is, if the clock period be τ, data increases by A at intervals of τ, and when the data exceeds a dynamic range D, it overflows. As the result, a saw-tooth wave data is obtained. As clear from FIG. 2, if the period of this saw-tooth waveform be T, the following relation holds:

$$T = D \cdot \tau / A \quad (1)$$

Supposing that the clock frequency be fc and the saw-tooth wave frequency fs (i.e. $fc = 1/\tau$ and $fs = 1/T$), Eq. (1) can be rewritten as:

$$fs = (A/D) \cdot fc \quad (2)$$

Thus, by changing the constant A and dynamic range D, the frequency of the saw-tooth waveform can be changed.

However, in general, the accumulating section 2 operates in binary notation, and in such event, D becomes an exponentiation of two. Thus, if fs is to be optionally set in accordance with Eq. (2), optional A must be given. However, since A is also an integer, an optional fs cannot be obtained.

The data generating section 2 is provided to solve this problem, and functions as follows. The data generating section 2 periodically generates a data string a period of m clocks (m is integer), and the total of the data string in each period is R (R is integer). Thus, the data average is R/m. Because the data having such average value is given to the accumulating section 1 always together with the constant A, the accumulating section is, on the average, equivalent to accumulating A + R/m value every clock. Consequently, substituting A in Eq. (2) for A + R/m gives

$$fs = \{(A + R/m)\}/D \cdot fc \quad (3)$$

Thus, proper selection of the integers R and m gives an optional frequency fs.

Eq. (3) can be also interpreted as follows. In Eq. (3), (A + R/m)/D denotes the ratio of to saw-tooth wave frequency fs to clock frequency fc, and if the ratio is expressed as k/h (where k and h are natural numbers and k/h the irreducible fraction), we obtain

$$k/h = (A + R/m)/D \quad (4)$$

Consequently, if the dynamic range D of the accumulating section 1 and the ratio k/h are given, A, R, and m can be obtained as follows:

$$k \cdot D/h = A + R/m \quad (5)$$

Thus, from Eq. (5), dividing $k \cdot D$ by h gives the quotient A with remainder R, and m is a denominator when $k \cdot D/h$ is reduced. For example, if D = 512, k = 3, and h = 22, from Eq. (5) the left member is $3 \times 512/22 = 768/11 = (69 \times 11 + 9)/11$

Thus, A = 69, R = 9, and m = 11.

Now, referring to FIG. 3, the second embodiment of the present invention is described hereunder. In FIG. 3 the accumulating section 3 comprises an adder 10 and a D-flip-flop 11 working as a delay circuit. Because the output of the adder 10 is delayed by one clock with the D-flip-flop 11 and returned to one input of the adder 10, the constant A inputted to another input of the adder 10 is

accumulated every clock. The adder 10 overflows when the accumulated valve exceeds D.

The adder 10 possesses a carry input, to which the output of the data generating section 4 is inputted.

The data generating section 4 of this embodiment comprises an adder 5, an overflow detector 6, a switching circuit 8, a subtraction circuit 7, and a D-flip-flop 9.

The adder 5 adds R to the output of the D flip-flop 9. The output of the adder 5 is checked by the overflow detector 6 if it exceeds m, and should it exceed m, the switching circuit 8 switches to its terminal 13 to subtract m from the output of the adder 5 with the subtractor 7. The output of the subtractor 7 is fed to the D-flip-flop 9. The output of the D flip-flop 9 is returned to the adder 5. The overflow detector 6 outputs "1" when detecting overflow and "0" otherwise to the carry input of the adder 10 in the accumulating section 3.

Because the above configuration is equivalent to accumulating R in the residual algebraic system with m as module, adding R by m times produces the same result. That is, the output data of the adder 5 has a cycle m, and the overflow detector 6 outputs "1" at the rate of R times to m times. Consequently, the average of m times of outputs of the overflow detector 6 becomes R/m, and adding this signal to the carry input of the adder 10 in the accumulating section 3 can produce equivalent effect to that of the first embodiment. The present embodiment is advantageous in that it can utilize the carry input of the adder 10 because the output of the data generating section 4 is either "0" or "1", that is, 1 bit.

Now referring to FIG. 4, the third embodiment is described. In this embodiment, the accumulating section 3 is the same as that of the second embodiment, while the data generating section 20 comprises an m-counter 22 and a ROM 21. The m-counter 22 divides the clock frequency by m. Same as the second embodiment, the data generating section 20 is a circuit to output "1" at the rate of R times to m times. In the present embodiment, the output of the m-counter 22 is given to the address input of ROM 21. ROM 21 stores "1" in R addresses out of m addresses, and "0" in the remaining m-R addresses. This allows the third embodiment to perform the same operation as the first embodiment. Alternatively, if ROM 21 stores in advance a pattern to be obtained at the output of the data generating section 4 of the second embodiment, the third embodiment performs the same operation as the second embodiment.

Now, referring to FIG. 5, the fourth embodiment of the present invention is described. This embodiment is realized by adding a ROM 30 and a D/A converter 31 to the first embodiment. The output waveform of the accumulating section 1 is saw-tooth waveform as shown in the first embodiments. Therefore, if sinusoidal data is stored in advance in ROM 30 as shown in FIG. 6 and the output data of the accumulating section 1 is fed to the address input of ROM 30, the output data of ROM 30 becomes a sinusoidal waveform data. It is possible to convert this data with the D/A converter 31 to an analog sine wave. Storing an optional waveform data other than sine wave in ROM 30 allows an optional waveform to be produced.

Now, referring to FIG. 7, the fifth embodiment of the present invention is described. This embodiment is realized by adding a D/A converter 32 to the first embodiment, thereby providing an analog saw-tooth waveform.

Claims

1. A digital oscillation apparatus comprising:
data generating means driven by a clock signal having a frequency fc for periodically generating a data string with a period of m clocks, where m is an integer, the total value of the data string in each period being a constant R, where R is an integer; and
accumulating means driven by the clock signal and having a dynamic range D, where D is an integer, for accumulating each data string generated by said data generating means and a constant A, wherein A is an integer, to obtain an accumulated data until the accumulated data exceeds the dynamic range D subtracting the dynamic range D form the accumulated data when the accumulated data exceeds the dynamic range D, thereby generating a periodic waveform data having a frequency $fs = (A + R/m).fc/D$.

2. A digital oscillation apparatus according to claim 1, wherein said data generating means generates, as the data string, data "1" in response to R clocks out of m clocks and data "0" in response to the remaining m-R clocks, and
wherein said accumulating means comprises:
delay means for delaying a data inputted thereto by one clock period; and adding means for adding the constant A, an output data of said delay means and, as a carry, the data generated by said data generating means, the added data being fed to said delay means and at the same being outputted as the accumulated data.

3. A digital oscillation apparatus according to claim 2, wherein said data generating means comprises: delay means for delaying a data inputted thereto by one clock period; and adding means for adding the constant D and an output data of said delay means, the added data being fed to said delay means, and for generating a carry data "1" when the added data exceeds m, the carry data being outputted as the data generated by said data generating means.

4. A digital oscillation apparatus according to claim 2, wherein said data generating means comprises: counting means for dividing the clock signal frequency by m; and memory means having stored therein data "1" in R addresses out of m addresses and data "0" in the remaining m-R addresses for outputting the

stored data, as the data generated by said data generating means, according to an output of said counting means received as an address data.

5. A digital oscillation apparatus according to claim 1, further comprising memory means having stored therein data corresponding to a predetermined waveform and receiving the waveform data from said accumulating means as an address data for outputting the stored data to obtain a predetermined periodic waveform data.

6. A digital oscillation apparatus according to claim 5, wherein said memory means has stored therein sinusoidal waveform data.

7. A digital oscillation apparatus according to claim 5, further comprising digital-to-analog conversion means for converting the waveform data from said memory means to an analog waveform signal.

8. A digital oscillation apparatus according to claim 1, further comprising digital-to-analog conversion means for converting the waveform data from said accumulating means to an analog waveform signal.

FIG. 1

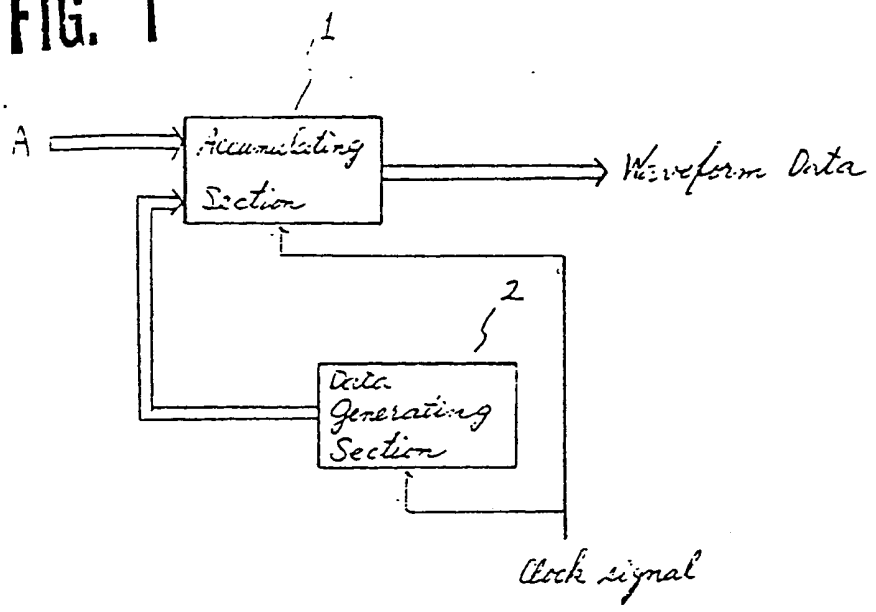

1
A
Accumulating Section
Waveform Data
2
Data Generating Section
Clock signal

FIG. 2

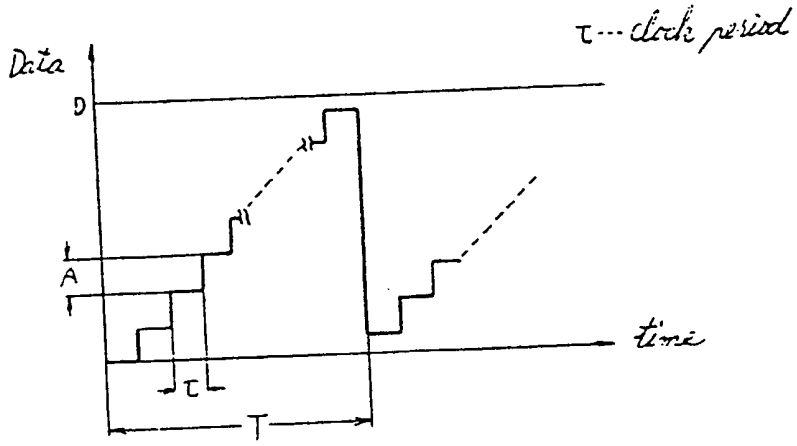

τ --- clock period
Data
D
A
time
τ
T

FIG. 3

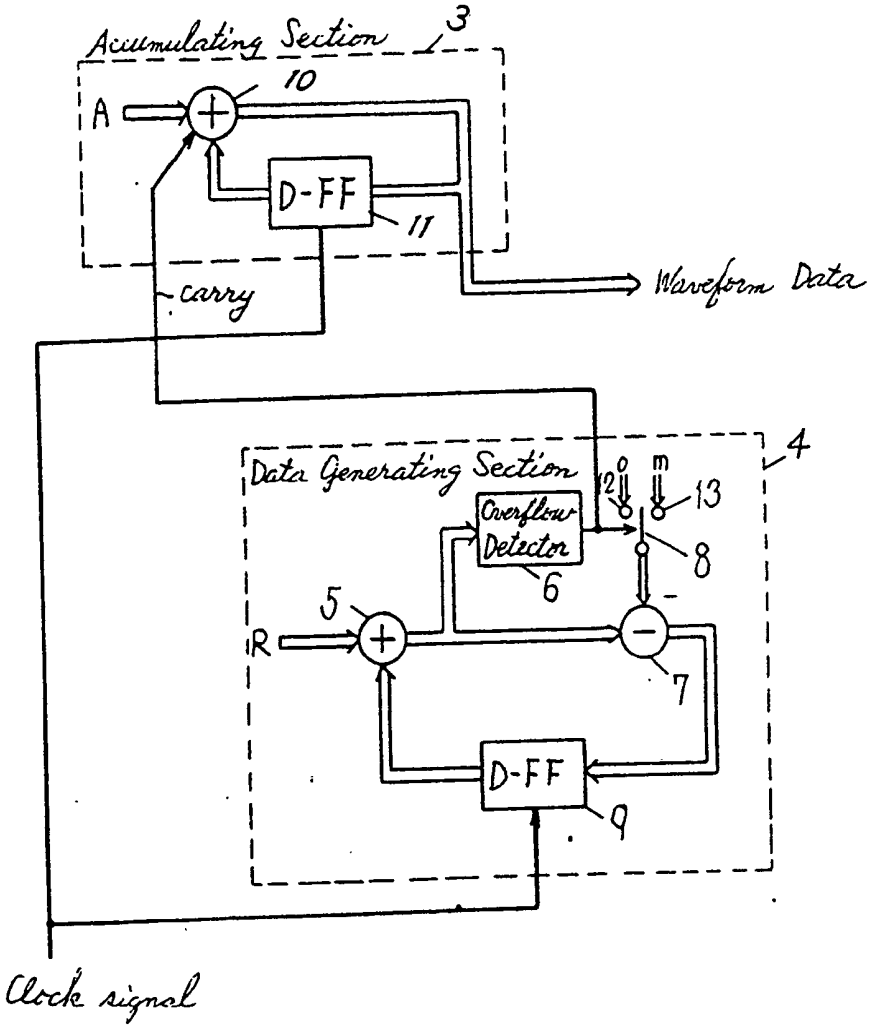


FIG. 4

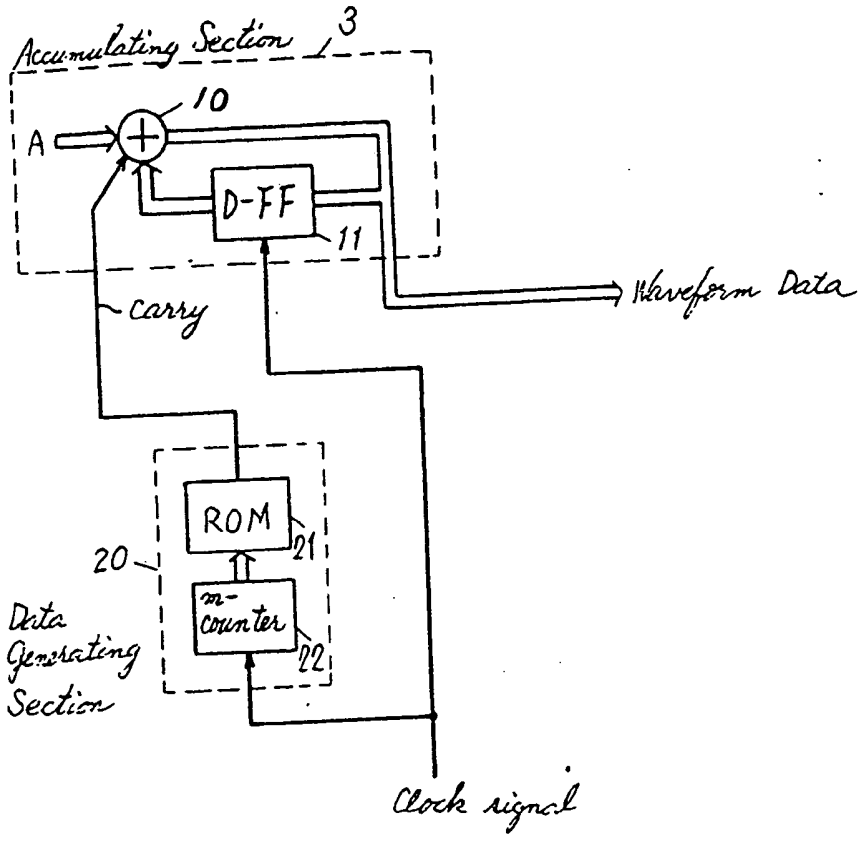

Accumulating Section
3
10
A
D-FF
11
Waveform Data
carry
ROM
21
20
m-counter
22
Data Generating Section
Clock signal

FIG. 5

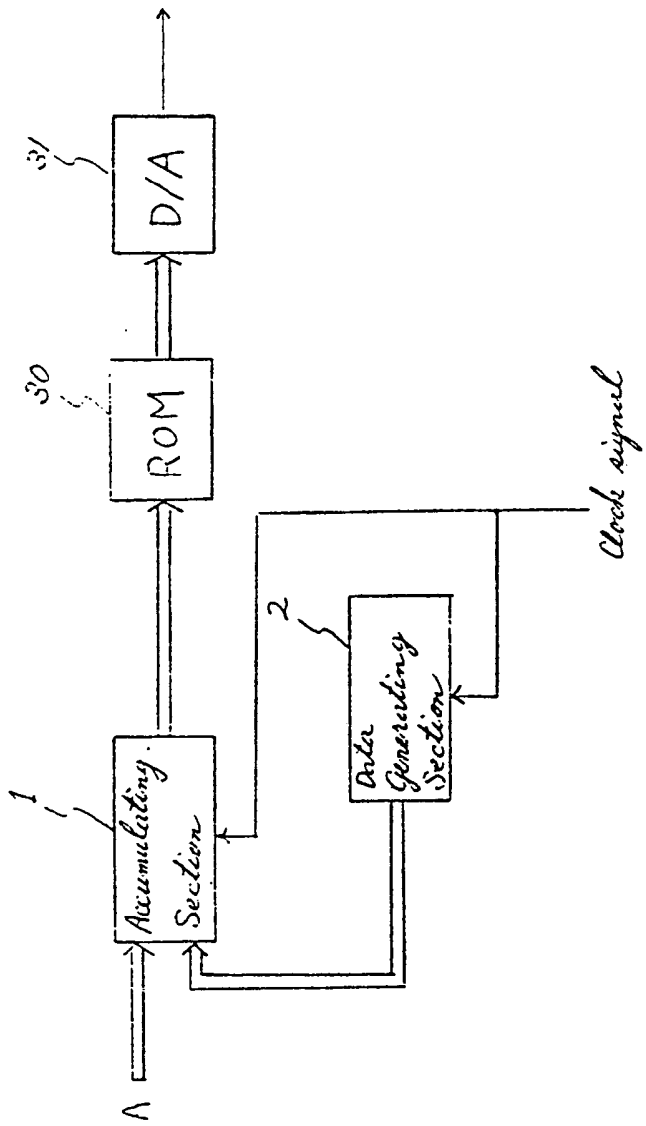

D/A
ROM
Accumulating Section
Data Generating Section
Clock signal
1
2
30
31

FIG. 6

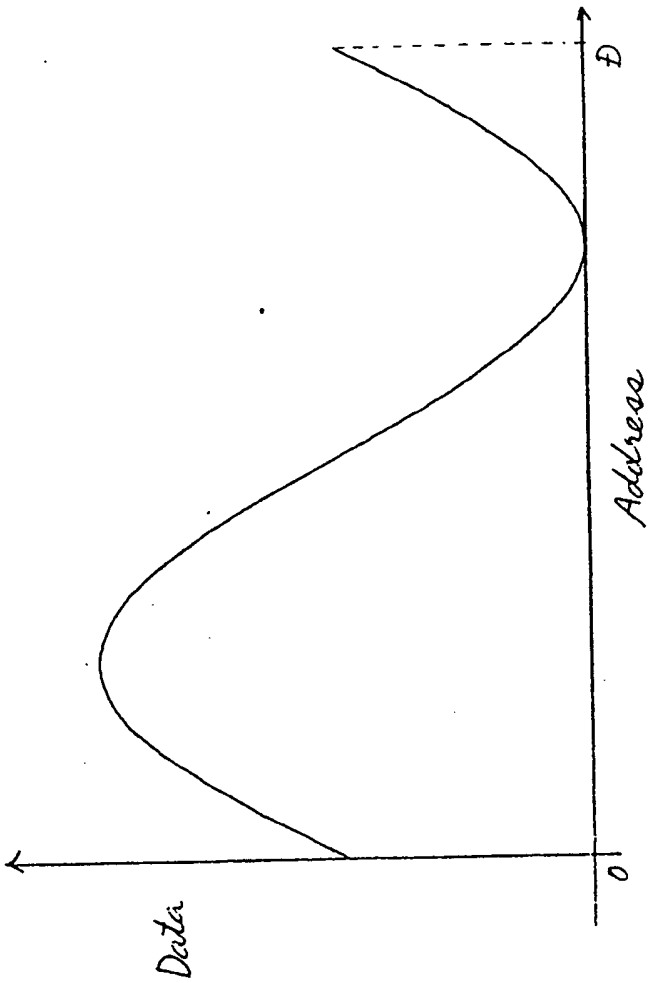
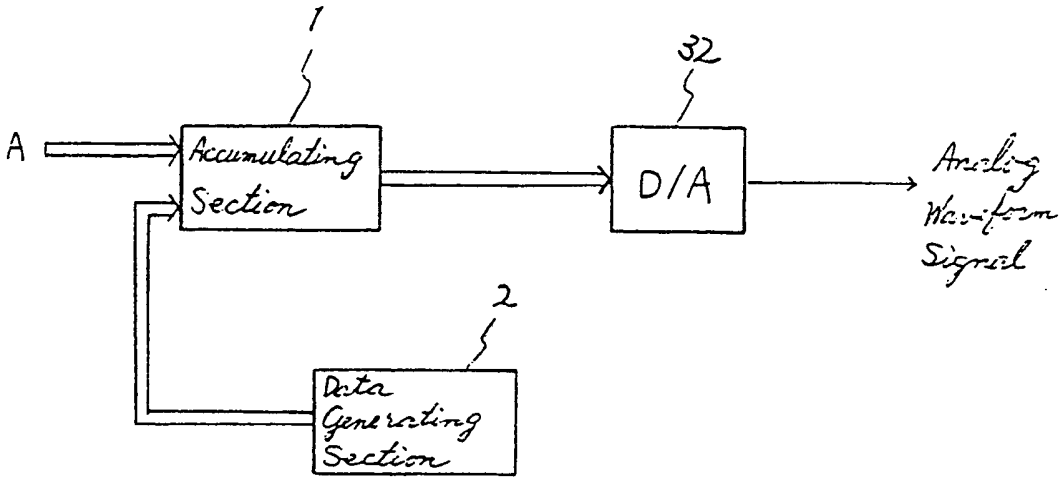


FIG. 7


1
32
A
Accumulating Section
D/A
Analog Waveform Signal
2
Data Generating Section

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(11) Publication number: **0 312 370 A3**

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(22) Date of filing: 13.10.88

(51) Int. Cl.[5]: G06F 7/548, G06F 7/60, G06F 1/02

(30) Priority: 13.10.87 JP 257556/87

(43) Date of publication of application:
19.04.89 Bulletin 89/16

(84) Designated Contracting States:
DE FR GB NL

(88) Date of deferred publication of the search report:
20.03.91 Bulletin 91/12

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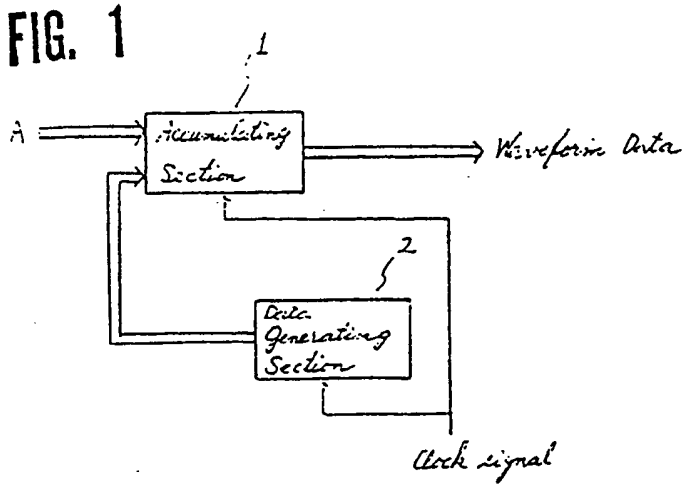
FIG. 1



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EUROPEAN SEARCH REPORT

Application Number

EP 88 30 9622

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 3, August 1979, pages 975-978, New York, US; J.E. SCHWAGER et al.: "Acoustic interactive synthesizer" * Figure; page 976, line 43 - page 977, line 17 *	1-8	G 06 F 7/548 G 06 F 7/60 G 06 F 1/02
Y	US-A-4 492 936 (ALBARELLO) * Abstract; figure *	1-8	
A	ELEKTRONIK, vol. 32, no. 17, August 1983, pages 51-52, Munich, DE; J. RISCHEWSKI: "Digitaler Funktionsgenerator" * Whole document *	5-7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 06 F H 03 K G 06 G

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	12 December 90	KHAZAM U.J.

CATEGORY OF CITED DOCUMENTS

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